1. A multi-layered circuit structure, comprising:

a first substrate having conductive via through holes disposed therein; and

a second substrate laminated to said first substrate and having conductive, adhesive-filled via through holes that align with, and make electrical contact with, the conductive via through holes of said first substrate upon lamination of said first and second substrates.

2. The multi-layered circuit structure in accordance with claim 1, wherein said first substrate comprises a signal core layer, and said second substrate comprises a power core layer.

3. The multi-layered circuit structure in accordance with claim 1, wherein said first substrate comprises a pair of outer signal core layers, and said second substrate comprises an inner power core layer sandwiched between said pair of outer signal core layers.

4. The multi-layered circuit structure in accordance with claim 3, wherein said via through holes of said inner power core layer comprise undercut contact surfaces, and said via through holes of said signal layer have metallic pads that make electrical contact with said undercut contact surfaces of said via through holes of said inner power core layer.

5. A multi-layered circuit structure, comprising:

a first substrate having conductive via through holes disposed therein; and

a second substrate laminated to said first substrate, and having via through holes comprising conductive adhesive coated pads that align with, and make electrical contact with, the conductive via through holes of said first substrate upon lamination of said first and second substrates.

6. The multi-layered circuit structure in accordance with claim 5, wherein said first substrate comprises a signal core layer, and said second substrate comprises a power core layer.

7. The multi-layered circuit structure in accordance with claim 5, wherein said first substrate comprises a pair of outer signal core layers, and said second substrate comprises an inner power core layer sandwiched between said pair of outer signal core layers.

8. A method of fabricating a multi-layered circuit, comprising the steps of:

filling via through holes of a first substrate with conductive adhesive;

aligning said via through holes of said first substrate with conductive via through holes of a second substrate; and

laminating together said first and second substrates.

9. The method in accordance with claim 8, wherein said first substrate comprises a signal core layer, and said second substrate comprises a power core layer.

10. The method in accordance with claim 8, wherein said first substrate comprises a pair of outer signal core layers, and said second substrate comprises an inner power core layer sandwiched between said pair of outer signal core layers.